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09/466,964	12/20/1999	GAD S. SHEAFFER	2207/7533	1789

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EXAMINER
NGUYEN, MIKE

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/466,964	Applicant(s) SHEAFFER, GAD S.
	Examiner Mike Nguyen	Art Unit 2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *01/19/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-30 are pending for the examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bitner Haim (U.S. Pat. No. 5,210,829).

4. As to claim 1, Bitner teaches a method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value (see figure 1 element 34 and figure 2 and column 8 lines 10-20), the method comprising:

receiving an advance indication of a memory service interruption (see figure 5 elements 74, 76); and

based at least in part on the received advance indication of the memory service interruption, modifying the watermark to have a second watermark value different from the first watermark value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

5. As to claim 2, Bitner teaches the method of claim 1, wherein the memory buffer having a watermark has a below-watermark burst size with a first burst size value (see figure 2 and column 8 lines 10-20), the method further comprising:

based at least in part on the received advance indication of the memory service interruption, modifying the below-watermark burst size to have a second burst size value

different from the first burst size value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

6. As to claim 3, Bitner teaches the method of claim 1, wherein the indication of a memory service interruption includes an advance indication of a memory service interruption having a worst case latency to memory (see figure 5 elements 74, 76 and column 21 lines 1-16).

7. As to claim 4, Bitner teaches method of claim 1, wherein the second watermark value is greater than the first watermark value (see figures 2, 3 element "BUFFER LEVEL", wherein the second watermark value is 430 Kb and the first watermark value is 0 Kb).

8. As to claim 5, Bitner teaches the method of claim 2 wherein the second burst size value is less than the first burst size value (see figures 2, 3 wherein the first burst size value is 500 Kb (500 Kb-0 Kb) and the second burst size value is 70 Kb (500 Kb-430 Kb)).

9. As to claim 6, Bitner teaches the method of claim 2 wherein the second burst size value corresponds to difference between the number of data entries in the memory buffer and the second watermark value (see figure 3 and element "BUFFER LEVEL", wherein the second burst size value is difference between the maximum capacity of buffer 34 and second watermark value 430 Kb).

10. As to claim 7, Bitner teaches the method of claim 1, the method further comprising

receiving an indication of the termination of the memory service interruption (see figure 5 element 84); and

based at least in part on the received indication of the termination of the memory service interruption, modifying the watermark to have a third watermark value different from the second

watermark value (see figure 4 and column 21 lines 29-31 and figure 5 element 74, 80 and column 21 lines 16-31).

11. As per claims 8, and 12, Bitner teaches the method of claim 7, wherein the third watermark value equals the first watermark value (see column 21 lines 29-31, wherein the third watermark value is 0 Kb which equals the first watermark value).

12. As to claim 9, Bitner teaches the method of claim 2, the method further comprising

receiving an indication of the termination of the memory service interruption (see figure 5 element 84);

based at least in part on the received indication of the termination of the memory service interruption, modifying the watermark to have a third value different from the second watermark value (see figure 4 and column 21 lines 29-31 and figure 5 elements 74, 80 and column 21 lines 16-31); and

based at least in part on the received indication of the termination of the memory service interruption, modifying the below-watermark burst size to have a third burst size value different from the second burst size value (see column 21 lines 29-31).

13. As to claim 10, Bitner teaches the method of claim 9, wherein the third watermark value equals the first watermark value, and wherein the third burst size value equals the first burst size value (see column 21 lines 29-31 and column 8 lines 10-20).

14. As to claim 11, Bitner teaches a method to control the loading of a memory buffer, the memory buffer having a watermark with a first watermark value (see figure 1 element 34 and figure 2 and column 8 lines 10-20), the method comprising:

modifying the watermark to have a second watermark value prior to the occurrence of a memory service interruption, the second watermark value being different than the first watermark value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

modifying the watermark to have a third watermark value subsequent to the occurrence of the memory service interruption, the third watermark value being different than the second watermark value (see figure 4 and column 21 lines 29-31 and figure 5 elements 74, 80 and column 21 lines 16-31).

15. As to claim 13, Bitner teaches the method of claim 11, wherein the memory buffer having a watermark with a first watermark value has an below-watermark burst size with a first burst size value (see figure 2 and column 8 lines 10-20), the method further comprising:

modifying the below-watermark burst-size to have a second burst size value prior to the occurrence of a memory service interruption, the second burst size value being different than the first burst size value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

modifying the below-watermark burst size to have a third burst size value subsequent to the occurrence of the memory service interruption, the third burst size value being different than the second burst size value (see column 21 lines 29-31).

16. As to claim 14, Bitner teaches the method of claim 13, wherein the first burst size value is equal to the third burst size value (see column 21 lines 29-31 and column 8 lines 10-20).

17. As to claim 15, Bitner teaches an apparatus to control the loading of a memory buffer, comprising:

a memory buffer (see figure 1 element 34); and

a memory controller, coupled to said memory buffer (see figure 1 element 32), including

a watermark register (see figure 1 and column 7 lines 53-58, wherein buffer watermark is adjustable; such as 0 Kb buffer watermark or 430 Kb buffer watermark, therefore it is obviously the controller has a watermark register);

a first register, coupled to said watermark register, to store a first watermark value (see figure 1 elements 34, 26 and figure 2 and column 8 lines 10-20, wherein the first watermark value 0 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a first register); and

a second register, coupled to said watermark register, to store a second watermark value (see figure 1 elements 34, 26 and figure 3 and column 10 lines 30-43, wherein the second watermark 430 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a second register).

18. As to claim 16, Bitner teaches the apparatus of claim 15, wherein the memory controller includes:

a below-watermark burst size register (see figure 2 and column 8 lines 10-20);

a third register, coupled to said below-watermark burst size register, to store a first below-watermark burst size value (see column 21 lines 29-31); and

a fourth register, coupled to said below-watermark burst size register, to store a second below-watermark burst size value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

19. As to claim 17, Bitner teaches the apparatus of claim 15, wherein the memory controller is to:

receive an advance indication of a memory service interruption (see figure 5 elements 74, 76);

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

store the second watermark value in said watermark register (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

20. As to claim 18, Bitner teaches the apparatus of claim 16, wherein the memory controller is to:

receive an advance indication of a memory service interruption (see figure 5 elements 74, 76);

read the second watermark value from said second register based at least in part on the received advance indication of a memory service interruption (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

store the second watermark value in said watermark register (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43)

read the second below-watermark burst size value from said fourth register based at least in part on the received advanced indication of a memory service interruption (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

store the second below-watermark burst size value in said below-watermark burst size register (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

21. As to claim 19, Bitner teaches a system to process video signals, the system comprising:

a processor (see figure 1 element 36);

a memory, coupled to said processor (see figure 1 element 22);

a memory buffer, coupled to said memory (see figure 1 element 34); and

a memory controller, coupled to said memory buffer (see figure 1 element 32), including

a watermark register (see figure 1 and column 7 lines 53-58, wherein buffer watermark is adjustable; such as 0 Kb buffer watermark or 430 Kb buffer watermark, therefore it is obviously the controller has a watermark register);

a first register, coupled to said watermark register, to store a first watermark value (see figure 1 elements 34, 26 and figure 2 and column 8 lines 10-20, wherein the first watermark value 0 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a first register); and

a second register, coupled to said watermark register, to store a second watermark value (see figure 1 elements 34, 26 and figure 3 and column 10 lines 30-43, wherein the second watermark 430 Kb is stored in the tape drive 26; therefore, it is obviously the controller has a second register).

22. As to claim 20, Bitner teaches the system of claim 19, wherein the memory controller is to:

receive an advance indication of a memory service interruption (see figure 5 elements 74, 76);

read the second watermark value from said second register based at least in part or, the received advance indication of a memory service interruption (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43); and

store the second watermark value in said watermark register (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

23. As to claim 21, Bitner teaches a computer-readable medium storing a plurality of instructions to be executed by a processor to control a memory buffer having a watermark with a first watermark value and a below-watermark burst size with a first burst size value (see figure 1 elements 36, 40, 34 and figure 2 and column 8 lines 10-20), said plurality of instructions comprising instructions to:

receive an advance indication of a memory service interruption (see figure 5 elements 74, 76); and

based at least in part on the received advance indication of the memory service interruption, modify the watermark to have a second watermark value different from the first watermark value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

24. As to claim 22, the computer-readable medium of claim 21, further comprising instructions to:

based at least in part on the received advance indication of the memory service interruption, modify the below-watermark burst size to have a second burst size value different from the first burst size value (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

25. As to claim 23, Bitner teaches an apparatus comprising:

a memory buffer (see figure 1 element 34); and

a memory controller coupled to said memory buffer, said memory controller to operate in

a first mode maintaining a first level of buffering in said memory buffer and to switch to a second mode maintaining a second level of buffer that is higher than the first level of buffering in response to an advance indication of a memory service interruption (see figure 1 element 32 and figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

26. As to claim 24, Bitner teaches the apparatus of claim23 wherein said memory service interruption is a DRAM refresh operation (see figure 1 and column 6 lines 59-67).

27. As to claim 25, Bitner teaches the apparatus of claim 23 wherein said memory service interruption is a memory maintenance operation (see figures 4, 5, wherein the memory service interruption is used to adjust the watermark value)

28. As to claim 26, Bitner teaches the apparatus of claim 23 wherein said first mode has an associated first burst size (see figure 2 and column 8 lines 10-20) and said second mode has an associated second burst size (see figure 5 elements 74, 76 and figure 3 and column 10 lines 30-43).

29. As to claim 27, Bitner teaches the apparatus of claim 3 wherein said memory buffer is a video buffer to buffer a video stream retrieved from memory (see column 25 lines 14-19).

30. As to claim 28, Bitner teaches an apparatus comprising:

a video stream buffer (see figure 1 elements 34, 26 and column 25 lines 14-19, wherein the buffer 34 can be a video stream buffer because the tape drive 26 also be implemented in other electromechanical devices)

a memory controller to occasionally perform an operation causing a memory service interruption (see figure 5 elements 74, 76); and

control logic coupled to said video stream buffer to maintain a first level of buffering in a first mode and to maintain a higher level of buffering prior to said memory controller performing said operation causing said memory service interruption (see figure 1 element 32 and column 6 lines 59-67).

31. As to claim 29, Bitner teaches the apparatus of claim 28 wherein said operation is a DRAM refresh operation (see figure 1 element 32 and column 6 lines 59-67).

32. As to claim 30, Bitner teaches the apparatus of claim 29 further comprising a processor (see figure 1 element 36), wherein said processor, said video stream buffer, said memory controller, and said control logic are all integrated into a single integrated circuit (see figure element 32).

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

JEFFREY GAFFIN
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Mike Nguyen
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Group Art Unit 2182

08/21/2002